REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application. Further, Applicant thanks the Examiner for the courtesies extended in the telephonic Examiner Interview of February 22, 2005.

Disposition of Claims

Claims 1-11 are pending in the present application. Claims 1, 5, 10, and 11 are independent. The remaining claims depend, directly or indirectly, from claims 1, 5, 10, and 11.

Claim Amendments

Claims 1, 2, 5, 6, 7, 10, and 11 have been amended by way of this reply. No new matter has been added by way of these amendments, as support for these amendments may be found, for example, in Figure 5 of the present application and in paragraphs [0026]-[0028] of the present application. Applicant believes the included amendments do not require a new search, or at least simplify issues for appeal, and accordingly, applicant respectfully requests entry and favorable consideration thereof.

Rejection(s) under 35 U.S.C § 112

Claims 1-11 were rejected under 35 U.S.C. § 112 as being indefinite. Claims 1, 2, 5, 6, 10, and 11 have been amended in this reply clarify the present invention recited. Claims 3 and 7 have been cancelled by way of this reply. Thus, the rejections with respect to claims 3 and 7 are now moot. Accordingly, withdrawal of the rejections with respect to claims 3 and 7 is respectfully requested. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

Claim 1

Independent claim 1 was rejected as being unclear as to (i) how the bypass is different from the path transferring the data or what is the source and destination of the bypass, (ii) on what the generation of the sign bit is based, and (iii) what the function of the aligner is with respect to the data transferred.

As discussed in the Examiner Interview of February 22, 2005 and as shown in Figure 5 of the present application, two paths transfer data from SRAM **32** to aligner **38**. In the bypass **50**, candidate bits are selected from the data. From the candidate bits, a sign bit is generated using a select signal **90** from the select **56** (*see* Specification, paragraphs [0025]-[0026]). A signal **92** from the select **56** is used to arrange the data into proper order in the aligner. Upon completion of the arrangement of the data and the sign bit, the data is transferred to another element in the microprocessor (*see* Specification, paragraph [0029]). As a sign bit is generated ahead of processing the data and sign bit in the aligner, signed load latency may be reduced (*see* Specification, paragraph [0039]).

Independent claim 1 has been amended to clarify that a sign bit is generated in a bypass path, where the generating is comprises selecting a plurality of candidate bits from the data and generating the sign bit from the plurality of candidate bits dependent on a select signal. Independent claim 1 has additionally been amended to clarify that the generating of the sign bit occurs independent of propagation of data through the data path.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 1 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 1 is respectfully requested.

Claim 5

Independent claim 5 was rejected as being unclear as to (i) how the bypass is different from the path transferring the data or what is the source and destination of the bypass and (ii) what the function of the aligner is with respect to the data transferred.

Claim 5 has been amended to clarify that a bypass path comprises a sign multiplexer for selecting a plurality of candidate bits from the data in the cache memory and a real-sign multiplexer for selecting a sign bit from the plurality of candidate bits dependent on a select signal. Further, claim 5 has been amended to clarify that the sign bit is selected independent of propagation of data through the data path and that the aligner arranges the data and the signed bit into signed data and transfers the signed data to the another element. Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 5 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 5 is respectfully requested.

Claims 2 and 6

Claims 2 and 6 were rejected as being unclear as to what the choices of selection are. As discussed above, claims 1 and 5 have been amended to clarify that a plurality of candidate bits are selected from the data, and a sign bit is generated from the plurality of candidate bits. Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 2 (dependent from claim 1) and claim 6 (dependent from claim 5) are clear and not indefinite. Accordingly, withdrawal of the § 112 rejections of claims 2 and 6 is respectfully requested.

Claims 4, 8, and 10

Claims 4, 8, and 10 were rejected as being ambiguous that the sign bit is generated by selectively processing a part of the data that is transferred from the cache memory to an aligner.

As discussed above, claim 1 has been amended to clarify that the generating comprises selecting a plurality of candidate bits from the data and generating the sign bit from

the plurality of candidate bits. Further, as discussed above, claim 5 has been amended to clarify that the bypass path comprises a sign multiplexer for selecting a plurality of candidate bits from the data and a real-sign multiplexer for selecting a sign bit from the plurality of candidate bits. Claim 10 has been amended to clarify that a sign bit is generated in a bypass path, where the means for generating is dependent a select signal, and the means for generating the sign bit comprises a means for selecting a plurality of candidate bits from the data and a means for selecting the sign bit from the plurality of candidate bits.

Accordingly, it is now clear that the sign bit is generated in a bypass from plurality of candidate bits, which are selected from the data. Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 4 (indirectly dependent from claim 1), claim 8 (indirectly dependent from claim 5), and claim 10 are clear and not indefinite. Accordingly, withdrawal of the § 112 rejections of claims 4, 8, and 10 is respectfully requested.

Claim 11

Independent claim 11 was rejected as (i) being ambiguous that the sign bit is generated by selectively processing a part of the data that is transferred from the cache memory to an aligner and as (ii) being unclear as to what the inputs and outputs of the multiplexers are.

Independent claim 11 has been amended to clarify that a bypass path connects the cache memory to the aligner, where the data is transferred from the cache memory to the bypass path and where a sign bit is transferred to the aligner from the bypass path. Claim 11 has been further amended to clarify that a select component in the bypass path provides signals to select the sign bit for the data. The select component comprises a sign multiplexer for selecting a plurality of candidate bits from the data and a real-sign multiplexer for select the sign bit from the plurality of candidate bits.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 11 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 11 is respectfully requested.

Rejection(s) under 35 U.S.C § 102

Claims 1-11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,638,312 issued to Simone (hereinafter "Simone"). Independent claims 1, 5, 10, and 11 have been amended to clarify the present invention. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The present invention is directed to a method and apparatus for reducing signed load latency in a microprocessor (*see* Specification, Abstract). As the signing process consumes the most time in a data transfer, this process generally determines the latency of a system (*see* Specification, paragraph [0009]). To reduce the latency due to signing data, embodiments of the present invention use a bypass (50) to generate a sign bit for the data, and transfer the sign bit along the bypass (50) to an aligner (38) (*see* Specification, paragraph [0024]). Data is transferred on a data path, *separate* from the bypass (50) that is used to generate and transfer the sign bit, to the aligner (38) (*see* Specification, paragraph [0029]).

With reference to the exemplary embodiment of the present invention shown in Figure 5 of the present application, data is transferred from SRAM (32) to a sign multiplexer ("mux") (52), which is part of a bypass (50). At the sign mux (52), candidate bits are selected from the data dependent on a select signal (90). At the real-sign mux (54), a sign bit is then selected from one of 8 candidate bits by a select signal (36). From the real-sign mux (54), the sign bit is transferred to an aligner (38).

With further reference to Figure 5 of the present application, the data discussed above is also transferred from SRAM (32) to a stretcher (140), which is part of a data path. The

stretcher (140) may extend or shrink the data to adjust the timing during data transfer. After the timing is adjusted, the data is transferred to a multiplexer (34), which may select a part of the data using a signal (36) from the CPU (12).

With reference to Figures 5 and 8 of the present application, the sign bit from the bypass (50) and the data from the data path are arranged in proper order in an aligner (38), using a signal (92) from the select (56). After the arrangement is complete, the data is transferred into another element in the microprocessor (*see* Specification, paragraphs [0026]-[0029], Figure 5, Figure 8).

Accordingly, independent claim 1 of the present invention requires selecting a plurality of candidate bits from the data and generating the sign bit from the plurality of candidate bits.

Simone, in contrast to the present invention, does not disclose at least the limitations of the claimed invention discussed above. Simone is directed to a method and apparatus for generating a zero flag status signal in a microprocessor (*see* Simone, Abstract). Simone is further directed to aligning data and sign bits to a desired format in multiplexers (701-707) *within* load aligner (102). Unsigned data are inputted directly into the load aligner (102), where all information regarding the data and sign bits is processed (*see* Simone, col. 8, lines 34-37). Sign bits are selected directly from data bits which are input to the load aligner (102) (*see* Simone, Fig. 7).

In embodiments of the present invention, latency due to sign bit generation is reduced by generating a sign bit in a bypass path, which is separate from a data path, and sending the generated sign bit to an aligner. The sign bit is generated from a plurality of candidate bits, which are generated from the data. In stark contrast to the present invention, Simone completely

fails to contemplate aligning data with a sign bit that has been generated form a plurality of candidate bits outside of an aligner, prior to alignment.

As shown in Figure 6 of Simone, the aligner (102) contains a multiplexer controller (601) and a multiplexer circuit (602). A data format code and unaligned data signals are input to aligner (102) (*see* Simone, col. 8, lines 5-12). Sign signals are generated *internal* to the aligner (102), directly from data bits input to mux (7) (*see* Simone, Figure 7; col. 8, lines 12-26). As seen with further respect to Figure 8 of Simone, Simone teaches that sign extension occurs sequentially, *after* the data bits are reordered (*see* Simone, Figure 8; col. 11, lines 36-52). Accordingly, Simone in no way teaches generating a sign bit in a bypass and transferring a sign bit to an aligner from a bypass path, as required by the claimed invention.

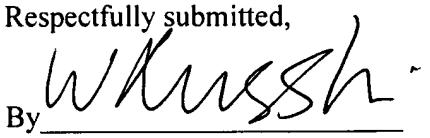
In view of the above, Simone fails to show or suggest the present invention as recited in independent claims 1, 5, 10, and 11. Thus, independent claims 1, 5, 10, and 11 are patentable over Simone. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/035001; P5030).

Dated: March 18, 2005

Respectfully submitted,

By 

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